CLAIMS

1. Flat thermionic emission screen (1) comprising a first substrate (2) on which are arranged an emission cathode (4) and an electron extraction grid (8), a second substrate (12) facing the first substrate (2), on which is arranged an anode (14) designed to collect the electrons emitted by the cathode(4), and an electronic control circuit (19) of the anode voltage (14) comprising at least one commutation component (18,20), characterized in that the commutation component (18,20) is integrated through design in the first substrate (2) and in the second substrate (12) of the screen (1).

2. Screen according to claim 1, characterized in that the said commutation component (18,20) is an HV transistor with a first electrode (40, 50) integrated in the first substrate(2), a second electrode (42,52) integrated in the second substrate (12) and a third electrode (44,54) integrated in the extraction grid (8).

3. Screen according to claim 1, characterized in that the anode (14) constitutes the emissive surface of the screen (1) and comprises at least one conducting surface (15) on which phosphor materials (17) are deposited.

4. Screen according to claim 2, characterized in that the cathode(4) comprises conducting columns (32) with sources of electrons (6), and in that the grid (8) comprises perforated conducting lines crossing the said

conducting lines at the positions of the said sources (6).

5.Screen according to claim 4, characterized in that the cathode (4) is a microtip source.

6. Screen according to claim 4, characterized in that the cathode (2) is a nanotube source.

Sub a2

7. Screen according to one of claims 1 to 6, characterized in that the electronic circuit (19) is of the push-pull type and comprises furthermore a second transistor (20) with a first electrode (50) integrated in the first substrate (2), a second electrode (52) integrated in the second substrate (12) and connected electrically to the first electrode (50) of the first transistor (18), and a third control electrode (54) integrated in the extraction grid (8) of the screen (1).

8. Screen according to one of claims 1 to 7, characterized in that it comprises furthermore a logical control module (100) comprising a low voltage source Vdd (24) and an optoelectronic coupler (26).

9. Screen according to claim 8, characterized in that the logical control module (100) comprises a load pump galvanically insulated from the screen (1) by a capacitor C.

10. Transistor, characterized in that it comprises a first semi-conducting substrate (80) on which are arranged a first electrode (40) and a control grid (44), a second substrate (86) facing the first substrate (80) and on which is arranged a second electrode (42) designed to collect the electrons emitted by the first electrode (40).

11. Transistor according to claim 10, characterized in that the first electrode (40) comprises microtips (6) arranged in lines and columns, the control grid (44) comprises perforated conducting lines crossing the columns of the first electrode (40) at the positions of the said microtips (6), the second electrode (42) comprises at least one conducting surface facing the said microtips (6).

add a3

Figure 3

HV Red anode voltage Time

HV Green anode voltage Time

HV Blue anode voltage Time

Figure 4

HV Anode voltage Image time Time

Figure 5

v1 Image time Time

v2 Image time Time

Figure 9

Ianode

$V(grid\text{-}cathode)_3$

$V(grid\text{-}cathode)_2$

$V(grid\text{-}cathode)_1$

$V(grid\text{-}cathode)_0$

$V(grid\text{-}cathode)_{SAT}$ $V(Anode\text{-}cathode)$